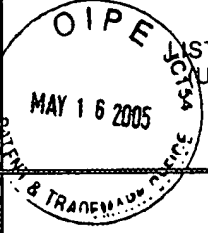
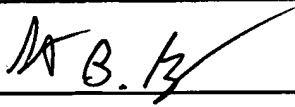


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| Form PTO-1449 | | U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | | ATTY. DOCKET NO. MI22-2357 | | SERIAL NO. 10/624,716 | |
|  LIST OF ART CITED BY APPLICANT (Use several sheets if necessary) | | | | APPLICANT Luan C. Tran | | | |
| | | | | FILING DATE July 21, 2003 | | GROUP 2812 | |
| U.S. PATENT DOCUMENTS | | | | | | | |
| *Examiner Initial | | Document Number | Date | Name | Class | Subclass | Filing Date If Appropriate |
| S.B.G. | AA | 5,534,456 | 07/96 | Yuan et al. | — | — | |
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| | | Document Number | Date | Country | Class | Subclass | Translation |
| | | | | | | | Yes No |
| S.B.G. | AP | JP04105328A | 04/92 | Japan | — | — | Abstract |
| / | AQ | | | | | | |
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| S.B.G. | AS | | Wolf et al., "Silicon Processing for the VLSI Era, Vol. 1: Process Technology," Second Edition, Lattice Press 2000, pp.12-13, 25-27. | | | | |
| S.B.G. | AT | | S.M. Sze, VLSI Technology, Second Edition, McGraw-Hill, 1988, pages 472-483 | | | | |
| EXAMINER | | | | DATE CONSIDERED | | | |
|  | | | | 3/30/06 | | | |
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| Application Number | 10/624.718 |
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| Filing Date | 07/21/2003 |
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| First Named Inventor | Luan C. Tran |
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| Art Unit | 2812 |
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| Examiner Name | J. Kennedy GYER |
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| Attorney Docket Number | MI22-2357 |
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Sheet 1 of 2

U. S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

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| Examiner Signature | <i>[Signature]</i> | Date Considered | 3-30-06 |
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| INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary) | | Complete if Known | |
| | | Application Number | 10/624,716 |
| | | Filing Date | July 21, 2003 |
| | | First Named Inventor | Luan C. Tran |
| | | Art Unit | 2812 |
| | | Examiner Name | J. Kennedy <i>Geyer</i> |
| Sheet 2 of 2 | Attorney Docket Number | M122-2357 | |

| NON PATENT LITERATURE DOCUMENTS | | | |
|---------------------------------|-----------------------|---|----------------|
| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T ² |
| <i>S.B.G.</i> | | Wolf et al., Silicon Processing for the VLSI Era, Volume 1-Process Technology, Second Edition, Lattice Press, 2000, pgs. 515-517. | |
| <i>S.B.G.</i> | | Wolf et al., Silicon Processing for the VLSI Era, Volume 1-Process Technology, Second Edition, Lattice Press, 2000, pgs. 527-531. | |
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| Examiner Signature | <i>L.B.G.</i> | Date Considered | 3-30-06 |
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